

<b>INFORMATION DISCLOSURE CITATION</b> PTO-1449		Customer Number: <b>26615</b>	ATTORNEY'S DKT NO. H1442		APPLICATION No. <del>Unassigned</del> 10/728, 910	
			APPLICANT(S) Wiley Eugene Hill et al.			
			FILING DATE December 8, 2003		GROUP <del>Unassigned</del> 2818	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
TH	4,996,574	02-26-91	Shirasaki	357	23.7	06-30-89
<b>FOREIGN PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes No
	}					
	}					
	}					
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
TH	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.					
}	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.					
}	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.					
}	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.					
TH	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.					
TH	Co-pending U.S. Application Serial No. 10/638,334, filed August 12, 2003, entitled: "Systems and Methods for Forming Dense N-Channel and P-Channel Fins Using Shadow Implantation," 16 page specification, 18 sheets of drawings.					
TH	Co-pending U.S. Application Serial No. 10/429,697, filed May 6, 2003, entitled: "FinFET-Based SRAM Cell," 16 page specification, 12 sheets of drawings.					
EXAMINER TH TH TH			DATE CONSIDERED Oct 04			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).